	Application No.	Applicant(s)
Notice of Allowability	10/767,426	UCHIDA ET AL.
	Examiner	Art Unit
	David E. Martinez	2181
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	6 (OR REMAINS) CLOSED in t) or other appropriate commur RIGHTS. This application is su	this application. If not included nication will be mailed in due course. THIS
1. This communication is responsive to 6/19/06.		
2. The allowed claim(s) is/are 1.3-9 and 11-16.		
 3. Acknowledgment is made of a claim for foreign priority u a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 3. Copies of the certified copies of the priority do International Bureau (PCT Rule 17.2(a)). * Certified copies not received: 	e been received. e been received in Application	No
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.		reply complying with the requirements
4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which giv	nitted. Note the attached EXAN es reason(s) why the oath or c	INER'S AMENDMENT or NOTICE OF declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must (a) including changes required by the Notice of Draftspers 1) hereto or 2) to Paper No./Mail Date (b) including changes required by the attached Examiner Paper No./Mail Date ldentifying indicia such as the application number (see 37 CFR 1 each sheet. Replacement sheet(s) should be labeled as such in the same contents.	son's Patent Drawing Review (- 's Amendment / Comment or it 1.84(c)) should be written on the	n the Office action of drawings in the front (not the back) of
 DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT 	OSIT OF BIOLOGICAL MATER FOR THE DEPOSIT OF BIOL	RIAL must be submitted. Note the OGICAL MATERIAL.
Attachment(s)		
Notice of References Cited (PTO-892)	5. Notice of Info	rmal Patent Application
2. Notice of Draftperson's Patent Drawing Review (PTO-948)	6. Interview Sun	
Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date		lail Date mendment/Comment
4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	9. 🗌 Other	FRITZ FLEMING SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Joseph Fox on 9/1/06. Examiner requested changes to amend the previously objected claims into the independent claims were agreed upon by the applicant on 9/1/06 to overcome a final rejection based on newly discovered prior art (US Patent Application Publication No. 2003/0182503 A1 to Leong et al.). Additional changes to the claims were also made by the applicant and agreed upon by the Examiner to further clarify the claims also to avoid a 112-2nd paragraph rejection. The claims submitted below are a clean version of the claims submitted by the proposed amendment of 9/1/06, attached hereto.

The application has been amended as follows:

The prior set of claims (claims 1-16) submitted on 6/19/06 have been replaced with the following claims:

- 1. A storage control apparatus for accessing data stored in a concatenation unit having a plurality of logical units, each logical unit being comprised of one or more physical units, by a request from a host, comprising:
 - a channel adapter for interfacing with said host; and
 - a plurality of controllers which control each one of the plurality of logical units,

wherein when said channel adapter receives said request from said host, said channel adapter sends an I/O data request for one logical unit of said plurality of logical units to a first controller which causes said one logical unit to execute I/O processing in said first controller,

and then said channel adapter sends another I/O data request for another logical unit of said plurality of logical units to a second controller which causes said another logical unit to execute I/O processing in said second controller, and

wherein said first controller judges whether said I/O data request is an I/O request extending over to said second controller which is in charge of said another logical unit after said I/O processing in said first controller, and sends a message indicative of the judgment result to said channel adapter.

Claim 2 has been cancelled.

3. The storage control apparatus according to Claim 1, wherein each controller has a table for storing the logical block address range of each logical unit, and

said first controller refers to said table in the logical block address range requested by said I/O data request, and judges whether said I/O data request is an I/O data request extending over to said second controller, which is in charge of said another logical unit.

- 4. The storage control apparatus according to Claim 1, wherein said channel adapter sends said I/O data request to said second controller according to the response from said first controller that the I/O data request extends to said second controller.
- 5. A storage control apparatus for accessing data stored in a concatenation unit having a plurality of logical units, each logical unit being comprised of one or more physical units, by a request from a host, comprising:
 - a channel adapter for interfacing with said host; and
 - a plurality of controllers which control each one of the plurality of logical units,

wherein when said channel adapter receives said request from said host, said channel adapter sends an I/O data request for one logical unit of said plurality of logical units to a first controller which causes said one logical unit to execute I/O processing in said first controller,

and then said channel adapter sends another I/O data request for another logical unit of said plurality of logical units to a second controller which causes said another logical unit to execute I/O processing in said second controller,

wherein said channel adapter has a table for storing said controllers corresponding to each logical unit, the logical block address range of each logical unit, and the logical units constituting said concatenation unit, and

said channel adapter selects a controller of said corresponding logical unit when said request is received from said host.

6. The storage control apparatus according to Claim 5, wherein each controller has a table for storing the logical block address range of each logical unit, and

said first controller refers to said table in the logical block address range requested by said I/O data request, and judges whether said I/O data request is an I/O data request extending over to said second controller, which is in charge of said another logical unit.

- 7. The storage control apparatus according to Claim 1, wherein said each controller comprises:
- a cache memory for storing a part of the data of said logical unit which the controller is in charge of; and
- a processing unit for executing I/O processing using said cache memory according to said I/O data request.
- 8. The storage control apparatus according to Claim 1, wherein said channel adapter is constituted by a plurality of channel adapters for connecting said plurality of controllers.
- 9. A storage control method for accessing data stored in a concatenation unit, each logical unit being comprised of one or more physical units, by a request from a host, comprising steps of:

Application/Control Number: 10/767,426

Art Unit: 2181

receiving said request from said host to a channel adapter;

sending an I/O data request for one logical unit of said plurality of logical units from said channel adapter to a first controller which is in charge of said one logical unit out of a plurality of controllers which are in charge of said plurality of logical units;

executing I/O processing in said first controller;

judging whether said I/O data request is an I/O data request extending over to said second controller which is in charge of said another logical unit after said I/O processing by said first controller;

sending a message indicative of the judgment result to said channel adapter,

sending another I/O data request for another logical unit of said plurality of logical units from said channel adapter to a second controller which is in charge of said another logical unit of said plurality of controllers which are in charge of said plurality of logical units; and

executing I/O processing in said second controller.

Claim 10 has been cancelled.

11. The storage control method according to Claim 9, wherein said response step comprises:

a step of referring to a table storing the logical block address range of each logical unit in the logical block address range requested by said I/O data request by said first controller; and

a step of judging whether said I/O data request is an I/O data request extending over to said second controller, which is in charge of said another logical unit.

12. The storage control method according to Claim 9, wherein the step of executing I/O processing in said second controller further comprises a step of sending said I/O data request to said second controller according to the response from said first controller that the I/O data request extends to said second controller by said channel adapter.

Application/Control Number: 10/767,426

Art Unit: 2181

13. A storage control method for accessing data stored in a concatenation unit, each logical unit being comprised of one or more physical units, by a request from a host, comprising steps of:

receiving said request from said host to a channel adapter;

sending an I/O data request for one logical unit of said plurality of logical units from said channel adapter to a first controller which is in charge of said one logical unit out of a plurality of controllers which are in charge of said plurality of logical units;

executing I/O processing in said first controller;

sending another I/O data request for another logical unit of said plurality of logical units from said channel adapter to a second controller which is in charge of said another logical unit of said plurality of controllers which are in charge of said plurality of logical units; and

executing I/O processing in said second controller,

wherein said reception step comprises:

a step of referring to a table for storing said controllers corresponding to each logical unit, logical block address range of each logical unit, and logical units constituting said concatenation unit by said channel adapter; and

a step of selecting a controller of said corresponding logical unit when said request is received from said host.

14. The storage control method according to Claim 13, wherein said response step comprises:

a step of referring to a table storing the logical block address range of each logical unit in the logical block address range requested by said I/O data request by said first controller; and

a step of judging whether said I/O data request is an I/O data request extending over to said second controller, which is in charge of another logical unit.

15. The storage control method according to Claim 9, wherein the I/O processing step for said I/O data request further comprises a step of executing I/O processing using a cache memory for storing a part of the data of said logical unit which each controller controls according to said I/O data request.

16. The storage control method according to Claim 9, wherein said channel adapter is constituted by a plurality of channel adapters for connecting said plurality of controllers, and said reception step further comprises a step of which one of the plurality of channel adapters for connecting said plurality of controllers receives the request from said host.

Allowable Subject Matter

Claims 1, 3-9 and 11-16 allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

As per claims 1 and 9, the prior art of record, alone or in combination fails to teach or fairly suggest wherein when said channel adapter receives said request from said host, said channel adapter sends an I/O data request for one logical unit of said plurality of logical units to a first controller which causes said one logical unit to execute I/O processing in said first controller, and then said channel adapter sends another I/O data request for another logical unit of said plurality of logical units to a second controller which causes said another logical unit to execute I/O processing in said second controller, and

wherein said first controller judges whether said I/O data request is an I/O request extending over to said second controller which is in charge of said another logical unit after said I/O processing in said first controller, and sends a message indicative of the judgment result to said channel adapter.

As per claims 5 and 13, the prior art of record, alone or in combination fails to teach or fairly suggest wherein when said channel adapter receives said request from said host, said

Application/Control Number: 10/767,426

Art Unit: 2181

channel adapter sends an I/O data request for one logical unit of said plurality of logical units to a first controller which causes said one logical unit to execute I/O processing in said first controller, and then said channel adapter sends another I/O data request for another logical unit of said plurality of logical units to a second controller which causes said another logical unit to execute I/O processing in said second controller,

wherein said channel adapter has a table for storing said controllers corresponding to each logical unit, the logical block address range of each logical unit, and the logical units constituting said concatenation unit, and

said channel adapter selects a controller of said corresponding logical unit when said request is received from said host.

The newly found reference (US Patent Application Publication No. 2003/0182503 A1 to Leong et al.) fails to teach the above limitations and only teaches independently sending sequential I/O requests to access stored data [abstract, paragraphs 70, 73].

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2181

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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